

# MEMORY ARRAY UNIT

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## REVISION HISTORY

- 01- Initial Release 2/7/83 JRW
- 02- Delay Module & LED wiring changes 2/11/83 JRW
- 03- Bank Output Latch Control & RAS/CAS Address Swap & Add Pin Numbers 6/10/83 ATK
- 04- Changes Made To Reflect REV. 2 Boards 1/20/84 HGO
- B01- RELEASE TO MANUFACTURING 8/9/84 JRW
- C00- RELEASE TO MANUFACTURING 10/29/84 JRW

DEFINE  
X\_FIRST=0  
X\_STEP=SIZE

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DRAWING:	410-000102-300 REV C00	ENGR:	WEATHERFORD
REVISED:	Mon Oct 29 14:20:22 1984	PAGE:	MAU. 1

8

7

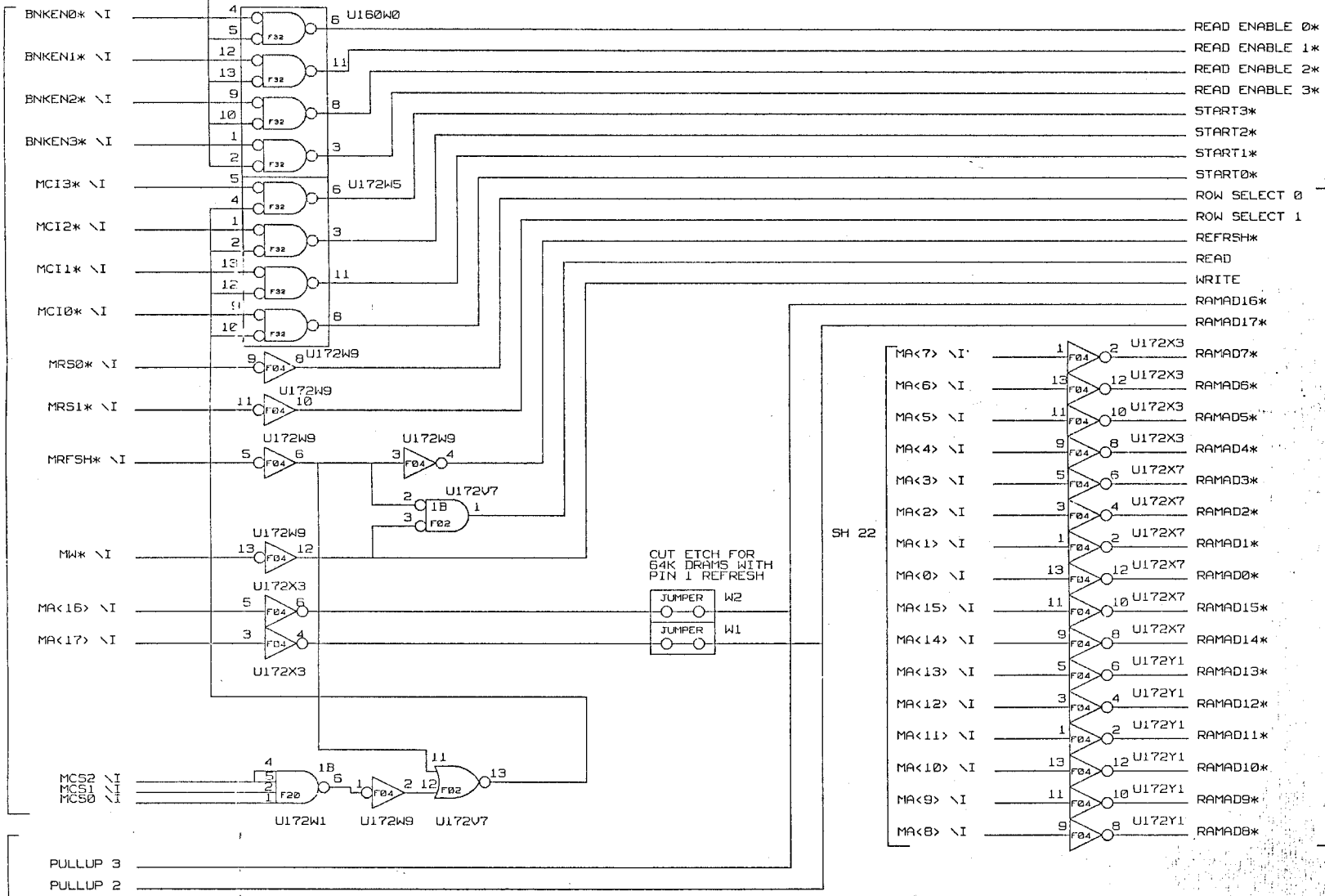
6

3

2

1

SH 20 ONLINE\*



SH 11 THRU 19

SH 6  
SH 5  
SH 4  
SH 3

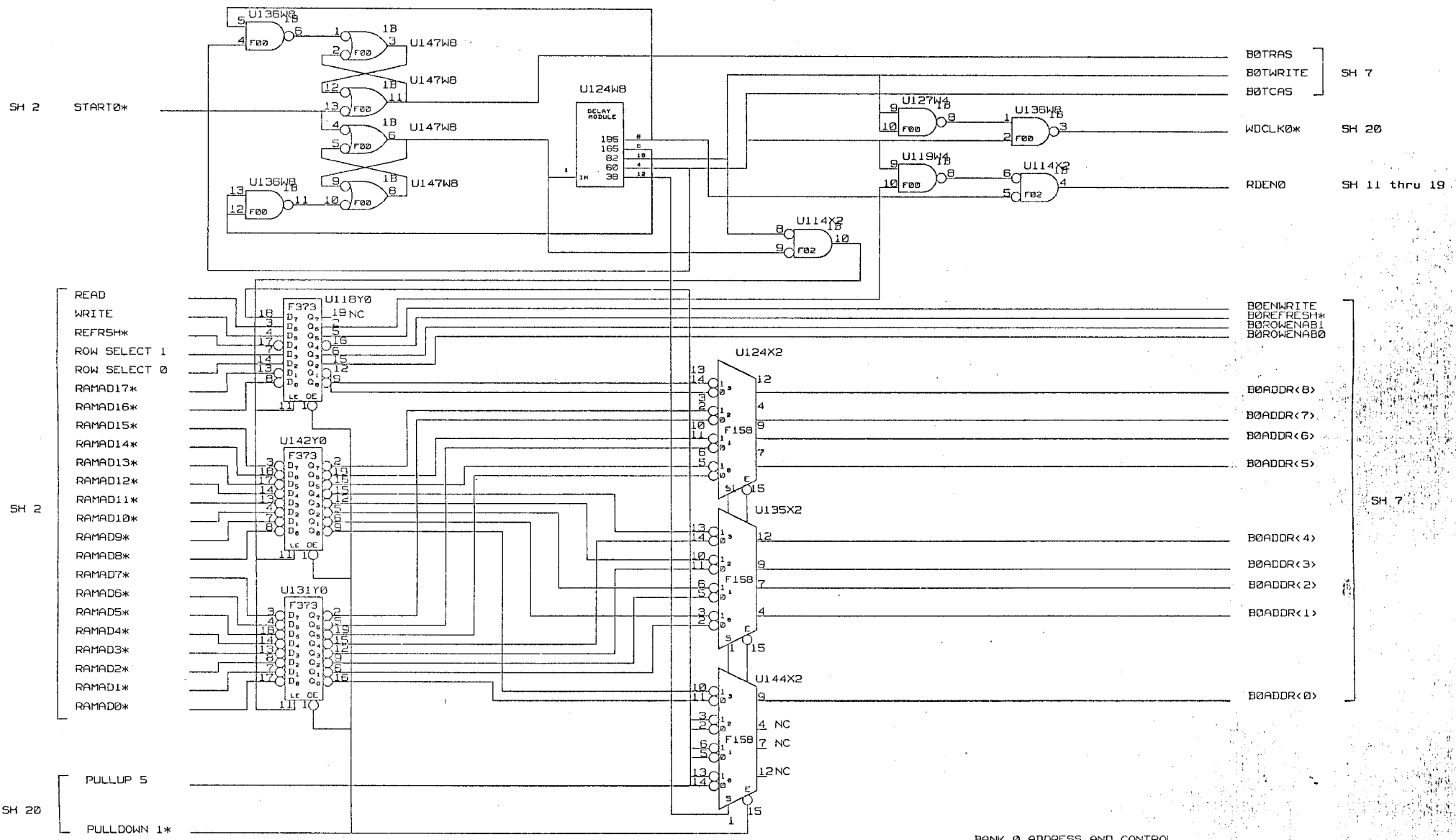
SH 3, 4, 5, 6

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REVISED: Thu Oct 11 20:35:11 1984	PAGE: MAU. 2

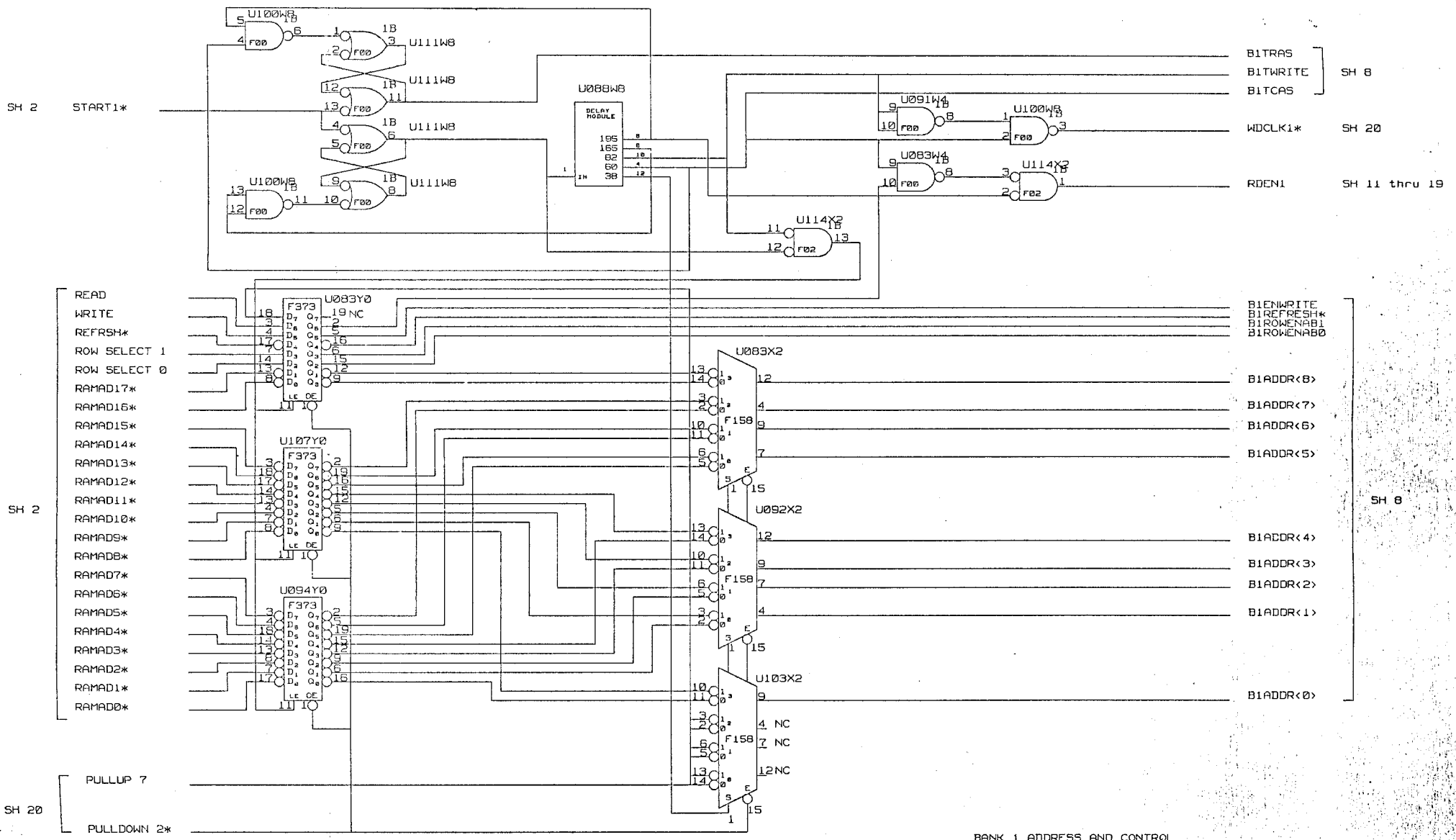


BANK 0 ADDRESS AND CONTROL

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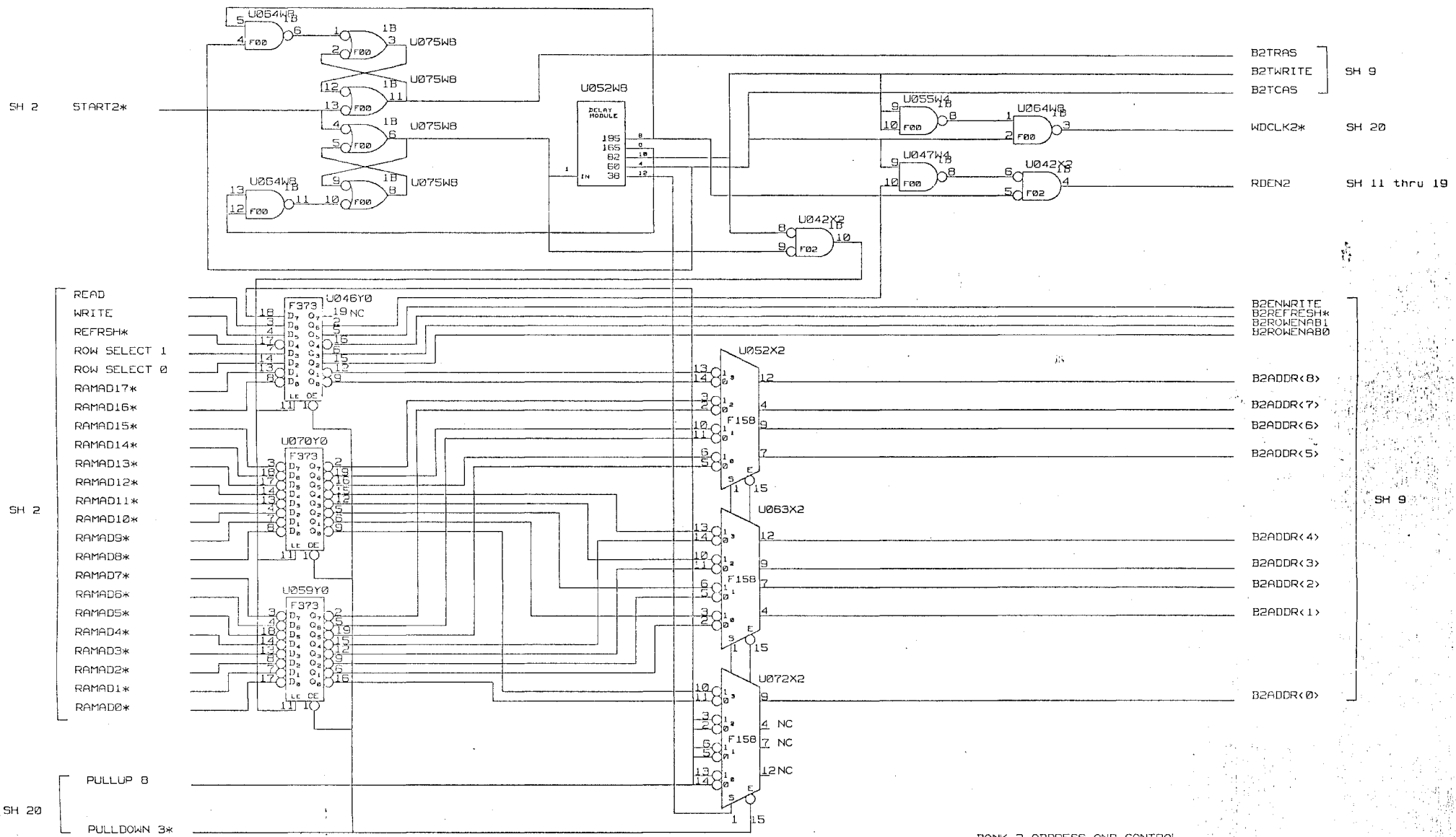
BANK 1 ADDRESS AND CONTROL

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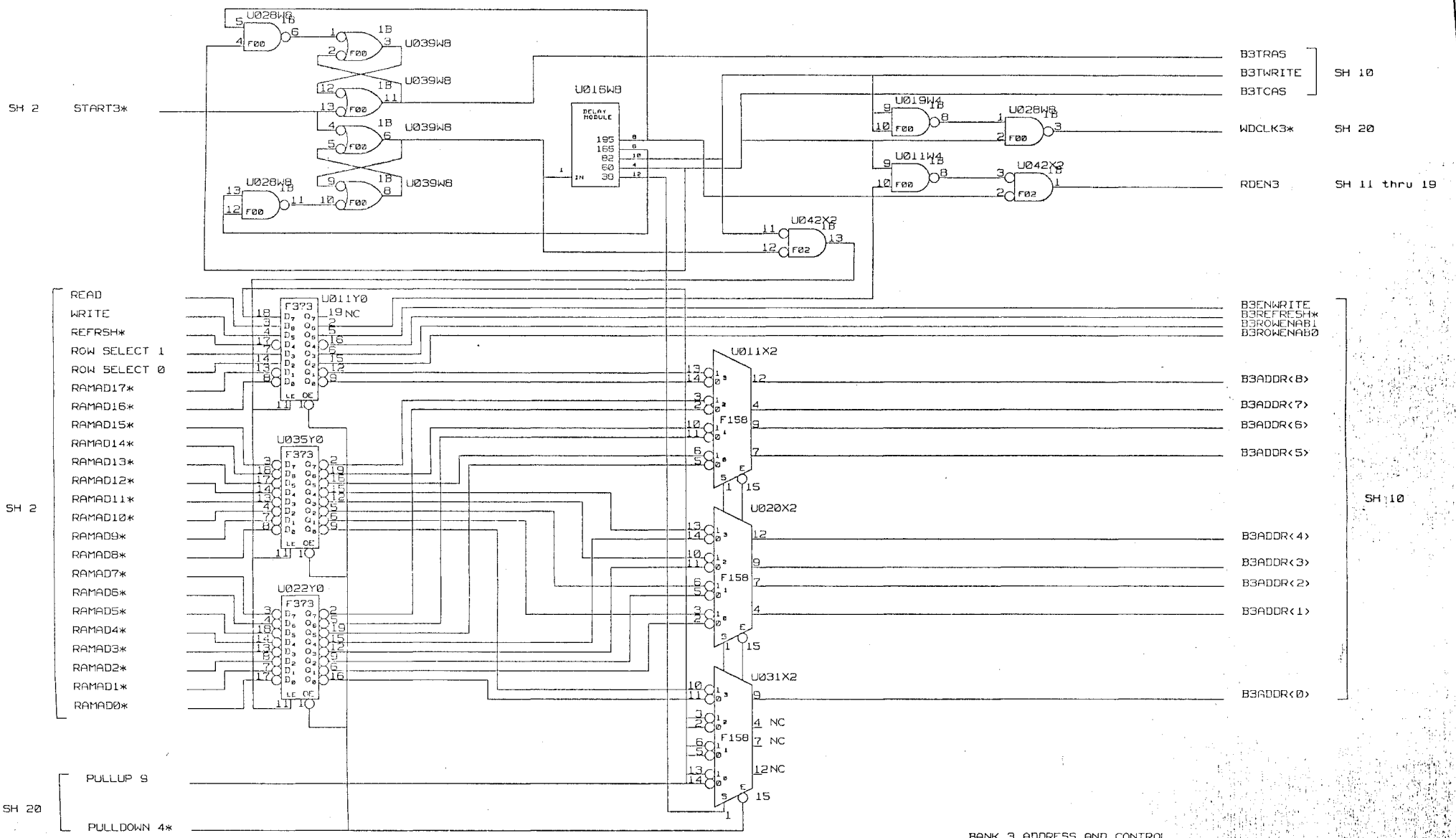


BANK 2 ADDRESS AND CONTROL

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DRAWING:	410-000102-300 REV C00	ENGR:	WEATHERFORD
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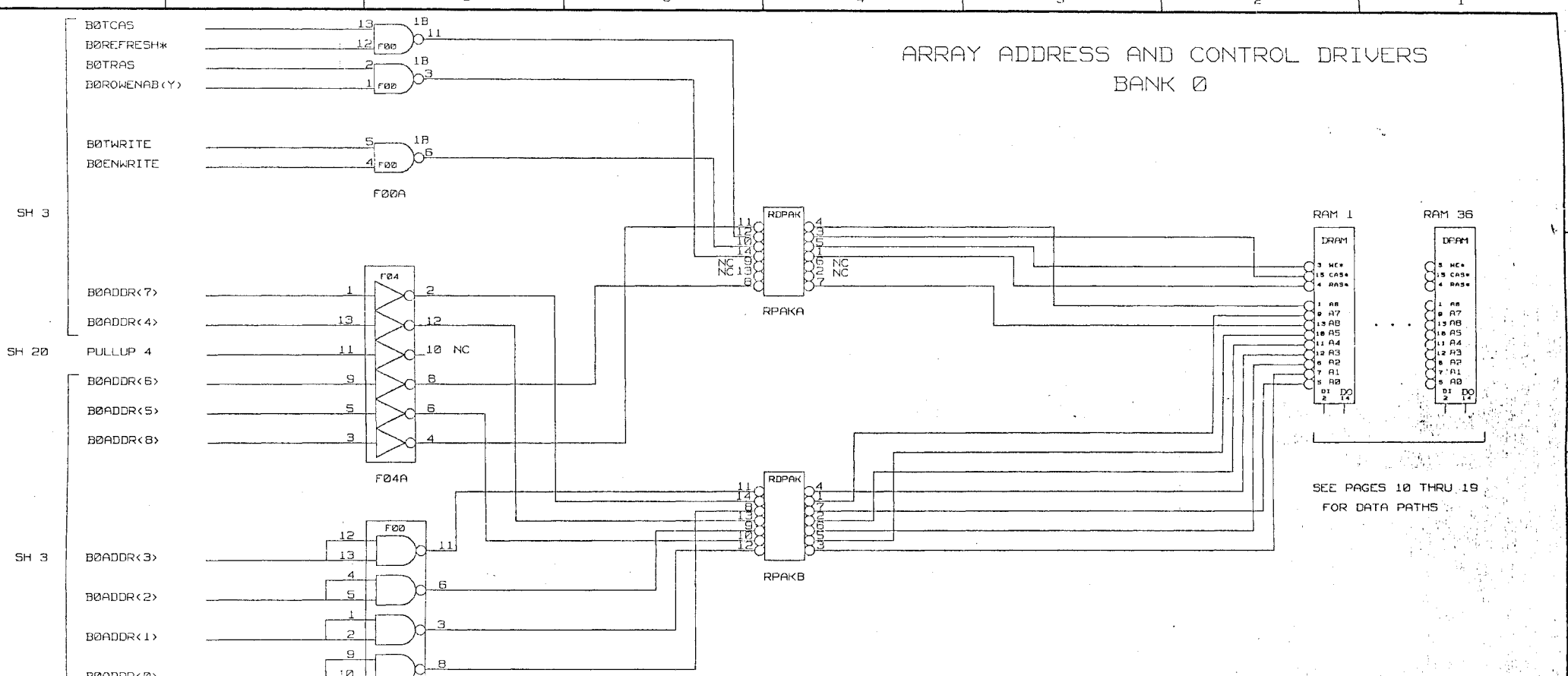
BANK 3 ADDRESS AND CONTROL

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# ARRAY ADDRESS AND CONTROL DRIVERS BANK 0



SEE PAGES 10 THRU 19  
FOR DATA PATHS

COL #	B0ROWENAB(Y)	F00A	F00B	F04	RPAKA	RPAKB	RAMS
142	B0ROWENAB(0)	U145W4	U145V2	U145W0	U145V6	U145T8	U143T1 U143S7 U143S3 U143R9 U143R5 U143R1 U143P7 U143P3 U143N9 U143N5 U143N1 U143M7 U143M3 U143L9 U143L5 U143L1 U143K7 U143K3 U143K0 U143J9 U143J5 U143J1 U143H7 U143H3 U143F9 U143F2 U143E7 U143E4 U143E0 U143D0 U143D6 U143D2 U143C6 U143C4 U143C0 U143B6 U143B2 U143A8
133	B0ROWENAB(1)	U137W4	U135V2	U135W0	U137V6	U137T8	U134T1 U134S7 U134S3 U134R9 U134R5 U134R1 U134P7 U134P3 U134N9 U134N5 U134N1 U134M7 U134M3 U134L9 U134L5 U134L1 U134K7 U134K3 U134K0 U134J9 U134J5 U134J1 U134H7 U134H3 U134F9 U134F2 U134E7 U134E4 U134E0 U134D0 U134D6 U134D2 U134C6 U134C4 U134C0 U134B6 U134B2 U134A8
124	B0ROWENAB(0)	U127W4	U127V2	U127W0	U127V6	U127T8	U125T1 U125S7 U125S3 U125R9 U125R5 U125R1 U125P7 U125P3 U125N9 U125N5 U125N1 U125M7 U125M3 U125L9 U125L5 U125L1 U125K7 U125K3 U125K0 U125J9 U125J5 U125J1 U125H7 U125H3 U125F9 U125F2 U125E7 U125E4 U125E0 U125D0 U125D6 U125D2 U125C6 U125C4 U125C0 U125B6 U125B2 U125A8
115	B0ROWENAB(1)	U119W4	U117V2	U117W0	U119V6	U119T8	U116T1 U116S7 U116S3 U116R9 U116R5 U116R1 U116P7 U116P3 U116N9 U116N5 U116N1 U116M7 U116M3 U116L9 U116L5 U116L1 U116K7 U116K3 U116K0 U116J9 U116J5 U116J1 U116H7 U116H3 U116F9 U116F2 U116E7 U116E4 U116E0 U116D0 U116D6 U116D2 U116C6 U116C4 U116C0 U116B6 U116B2 U116A8

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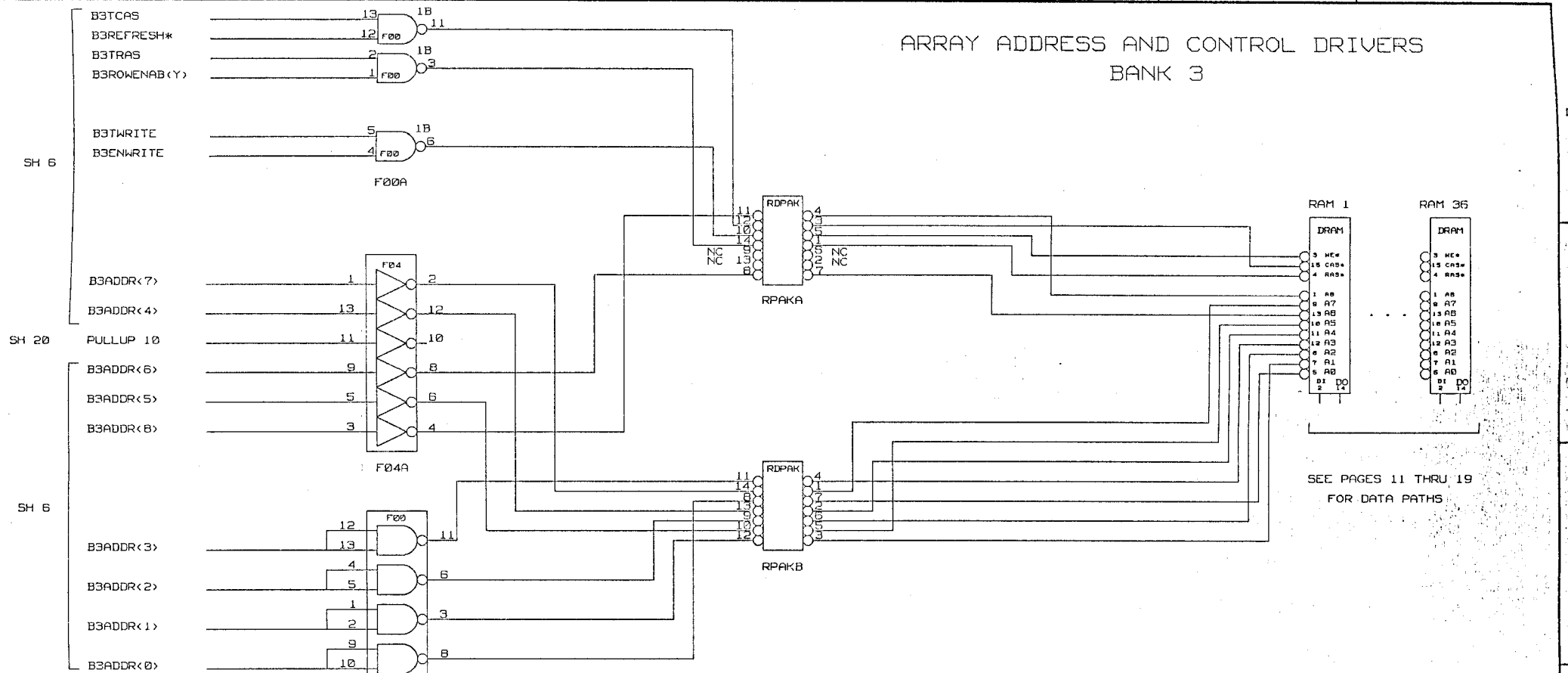


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### ARRAY ADDRESS AND CONTROL DRIVERS BANK 3



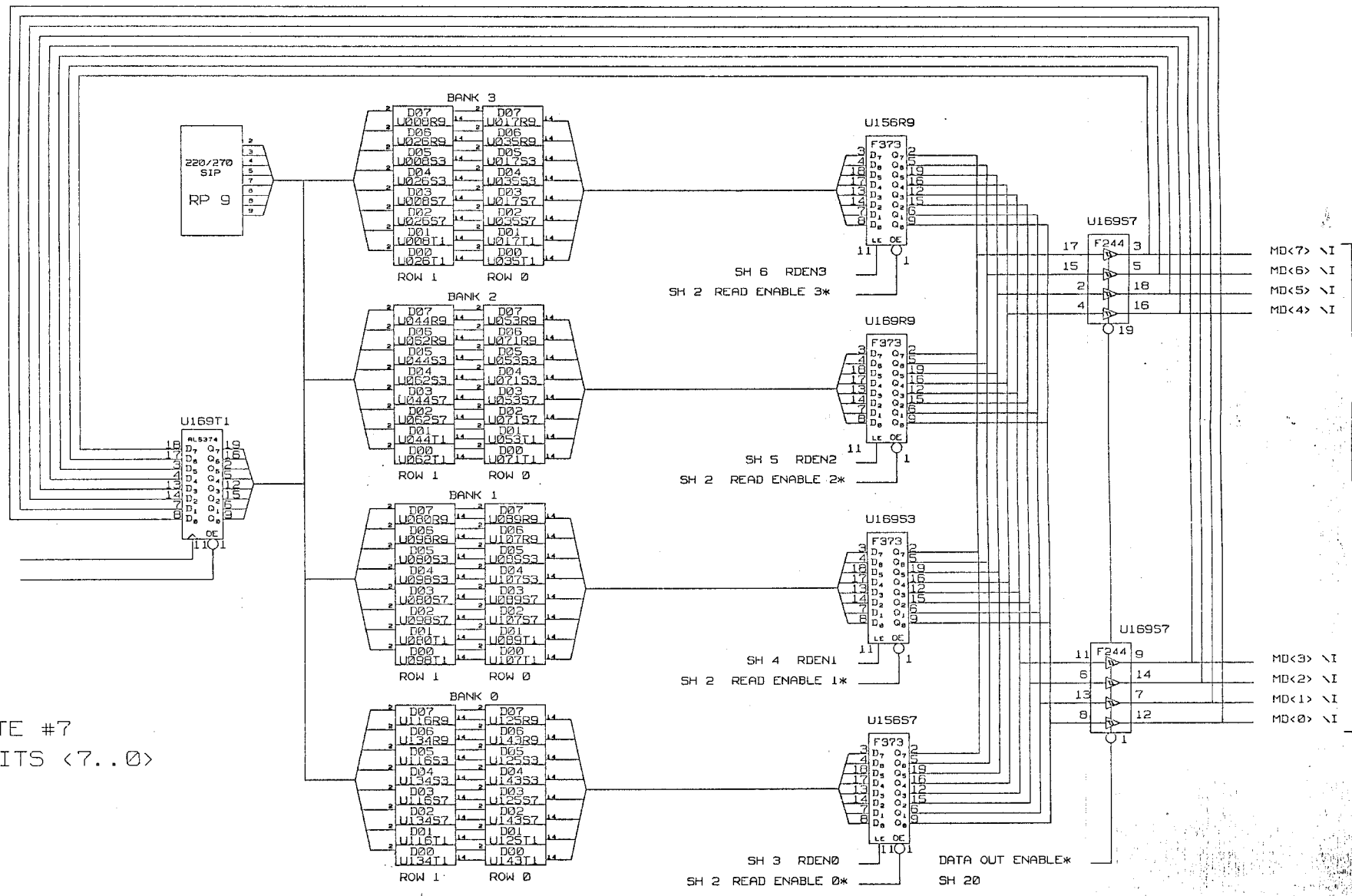
SEE PAGES 11 THRU 19  
FOR DATA PATHS

COL #	B3ROWENAB<Y>	F00A	F00B	F04	RPAKA	RPAKB	RAMS
034 BANK 3 ROW 0 EVEN DATA BITS	B3ROWENAB<0>	U037W4	U037V2	U037W0	U037V6	U037T8	U035T1 U03557 U03553 U035R9 U035R5 U035R1 U035P7 U035P3 U035N9 U035N5 U035N1 U035M7 U035M3 U035L9 U035L5 U035K7 U035K3 U035J9 U035J5 U035J1 U035H7 U035H3 U035F9 U035F5 U035E8 U035E4 U035E0 U035D6 U035D2 U035C8 U035C4 U035C0 U035B6 U035B2 U035A8
025 BANK 3 ROW 1 EVEN DATA BITS	B3ROWENAB<1>	U029W4	U029V2	U029W0	U029V6	U029T8	U026T1 U02657 U02653 U026R9 U026R5 U026R1 U026P7 U026P3 U026N9 U026N5 U026N1 U026M7 U026M3 U026L9 U026L5 U026K7 U026K3 U026J9 U026J5 U026J1 U026H7 U026H3 U026F9 U026F5 U026E8 U026E4 U026E0 U026D6 U026D2 U026C8 U026C4 U026C0 U026B6 U026B2 U026A8
016 BANK 3 ROW 0 ODD DATA BITS	B3ROWENAB<0>	U019W4	U019V2	U019W0	U019V6	U019T8	U017T1 U01757 U01753 U017R9 U017R5 U017R1 U017P7 U017P3 U017N9 U017N5 U017N1 U017M7 U017M3 U017L9 U017L5 U017K7 U017K3 U017J9 U017J5 U017J1 U017H7 U017H3 U017F9 U017F5 U017E8 U017E4 U017E0 U017D6 U017D2 U017C8 U017C4 U017C0 U017B6 U017B2 U017A8
007 BANK 3 ROW 1 ODD DATA BITS	B3ROWENAB<1>	U011W4	U009V2	U009W0	U011V6	U011T8	U008T1 U00857 U00853 U008R9 U008R5 U008R1 U008P7 U008P3 U008N9 U008N5 U008N1 U008M7 U008M3 U008L9 U008L5 U008K7 U008K3 U008J9 U008J5 U008J1 U008H7 U008H3 U008F9 U008F5 U008E8 U008E4 U008E0 U008D6 U008D2 U008C8 U008C4 U008C0 U008B6 U008B2 U008A8

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REVISOR: Thu Oct 11 20:29:41 1984  
PAGE: MAU.10



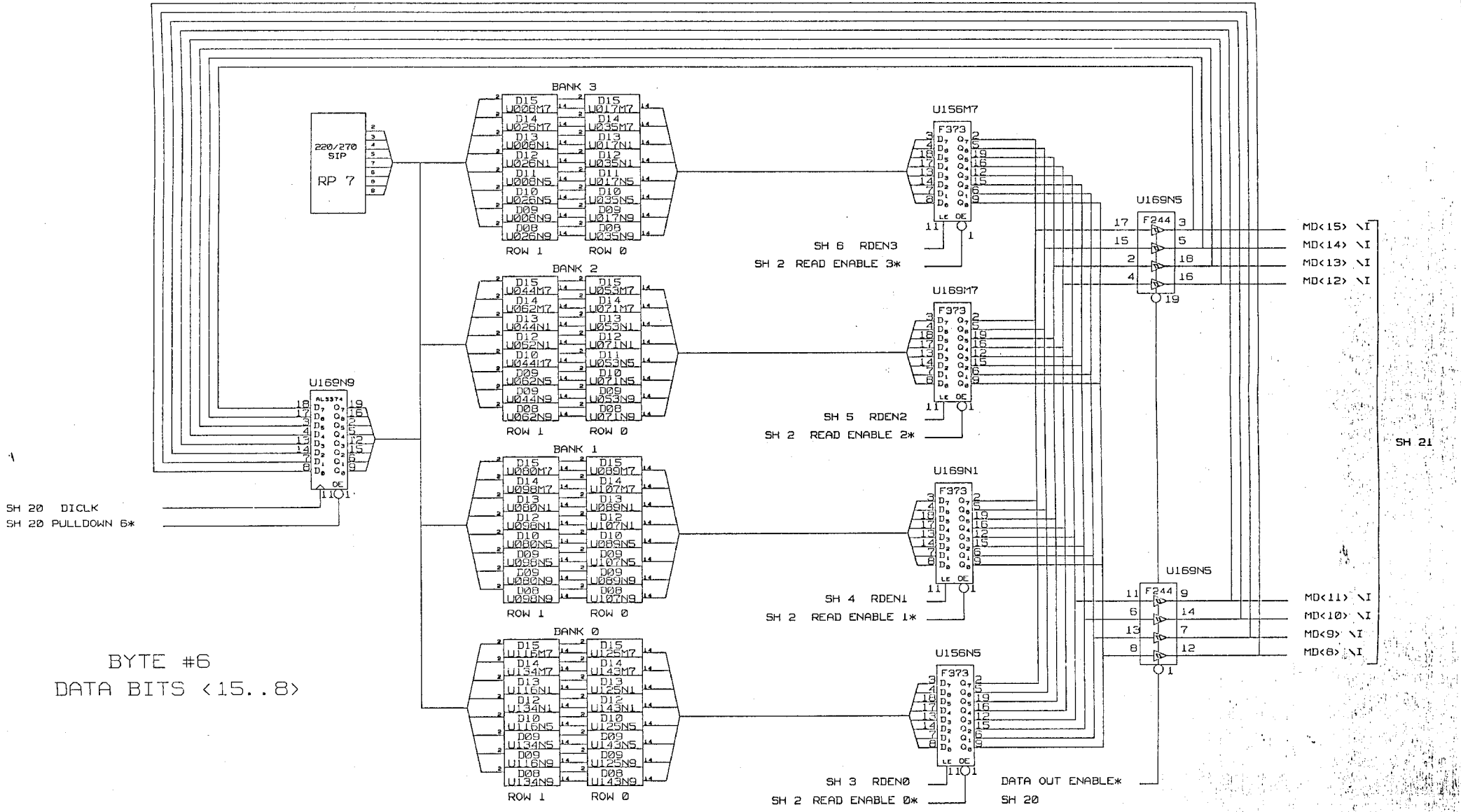
1 20 DICKL  
1 20 PULLDOWN 6\*

BYTE #7  
DATA BITS <7..0>

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SH 20 DICK  
SH 20 PULLDOWN 5\*

BYTE #6  
DATA BITS <15..8>

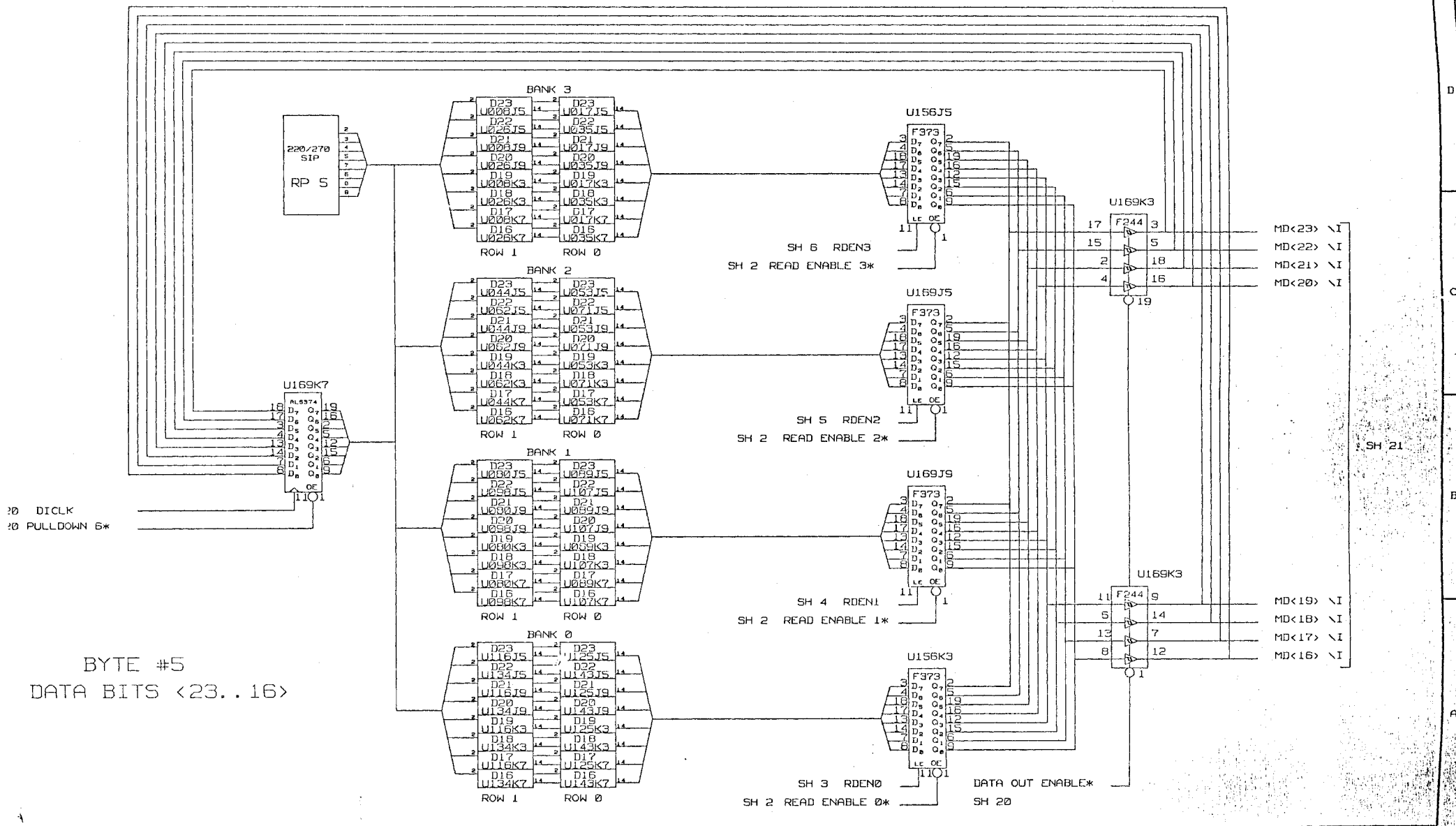
D  
C  
B  
A

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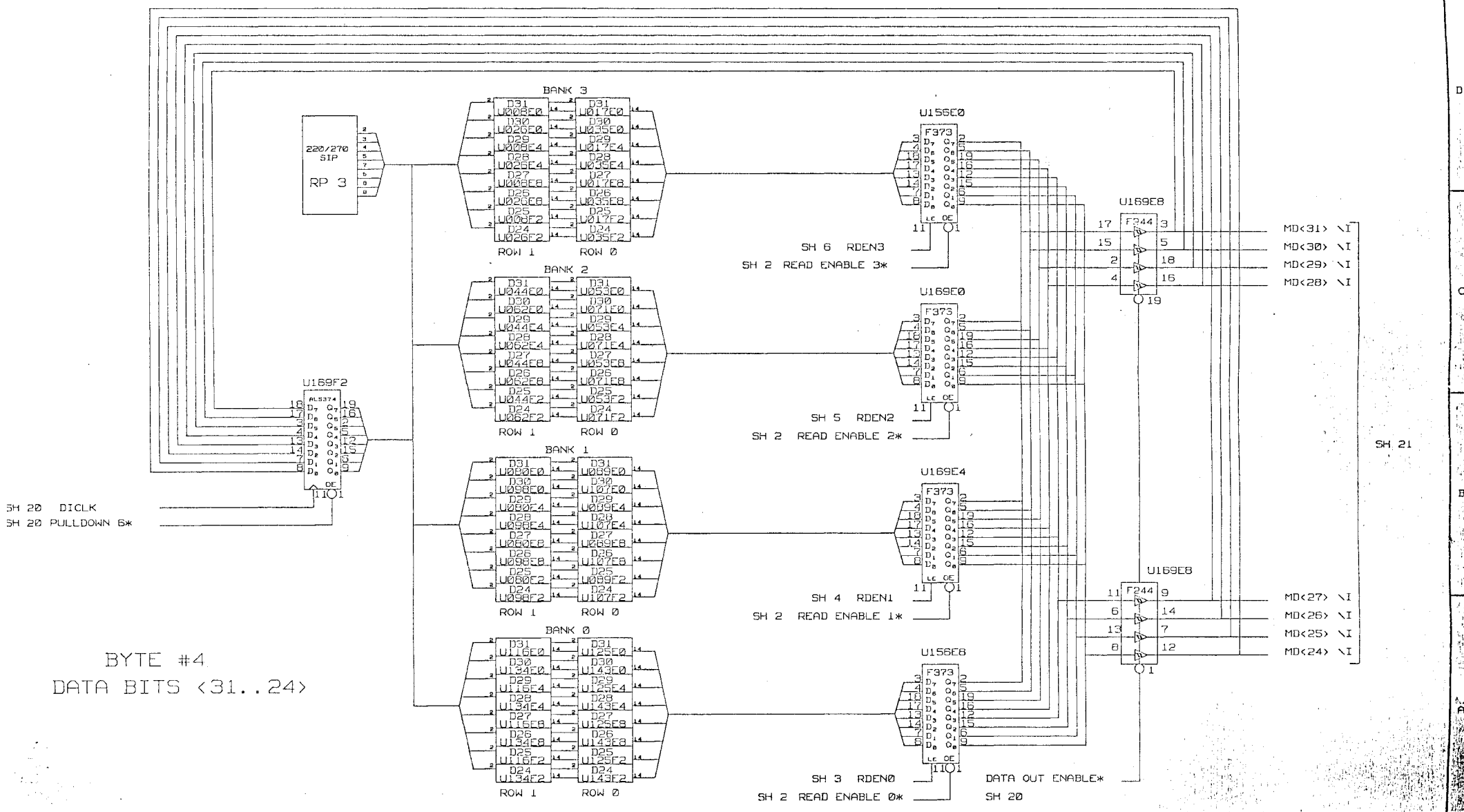
00 DICKL  
00 PULLDOWN 6\*

BYTE #5  
DATA BITS <23..16>

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REVISED:	Thu Oct 11 19:29:52 1984	PAGE:	MAU.13
3	2	1	



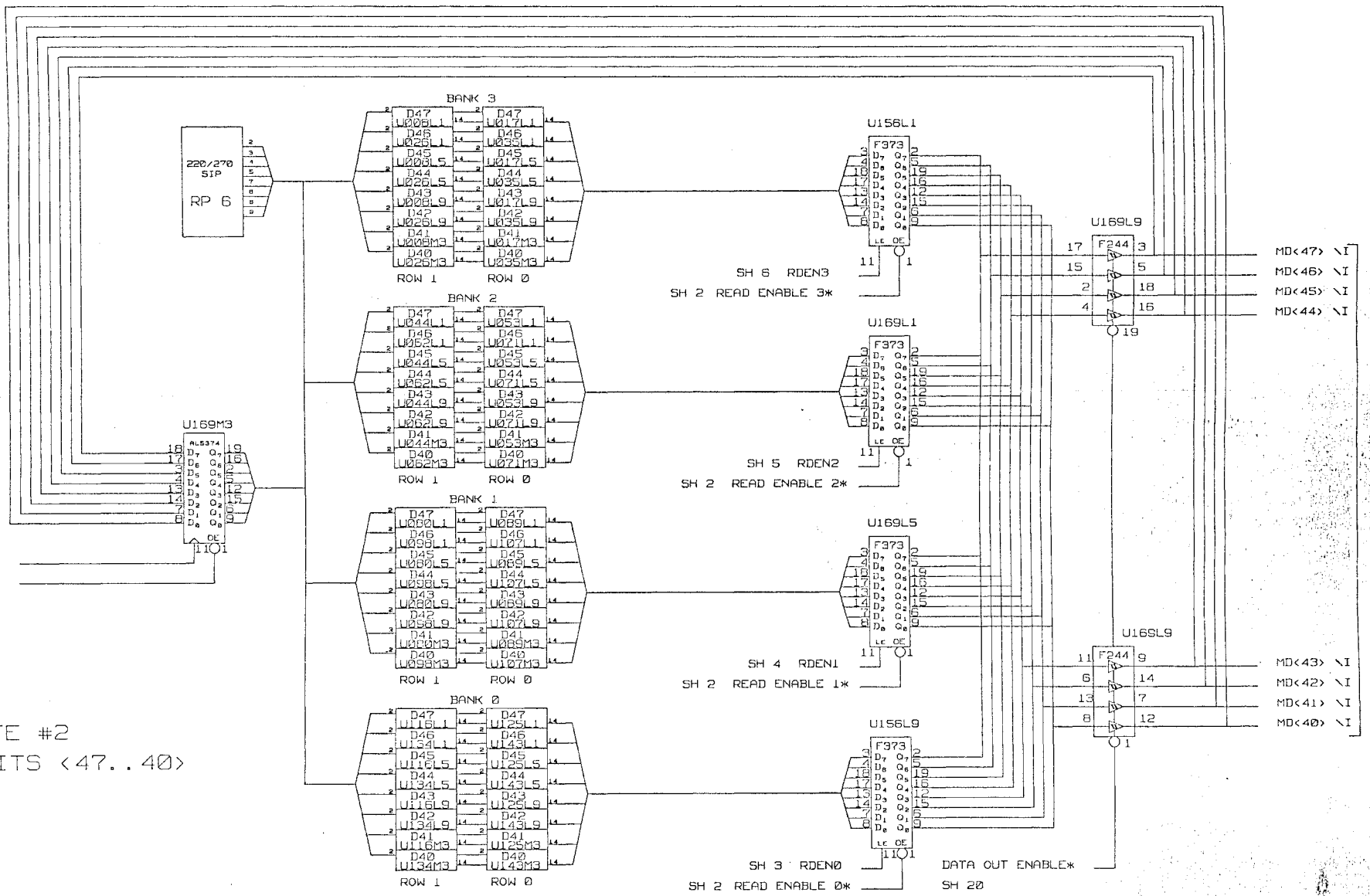
BYTE #4  
DATA BITS <31..24>

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SH 20 DI CLK  
SH 20 PULLDOWN 6\*

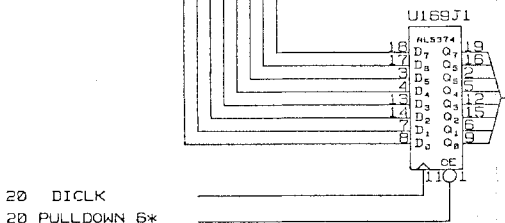
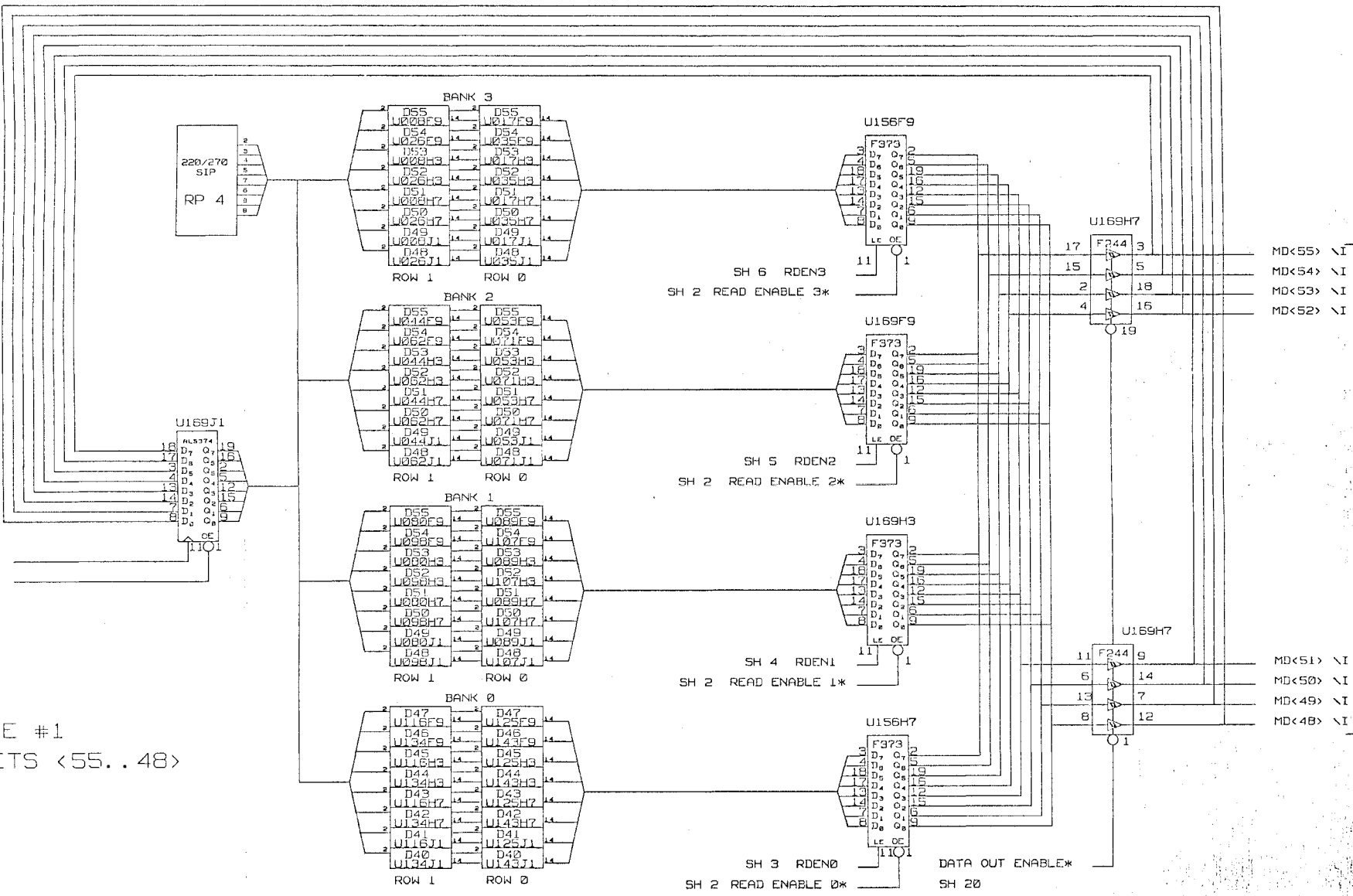
BYTE #2  
DATA BITS <47..40>

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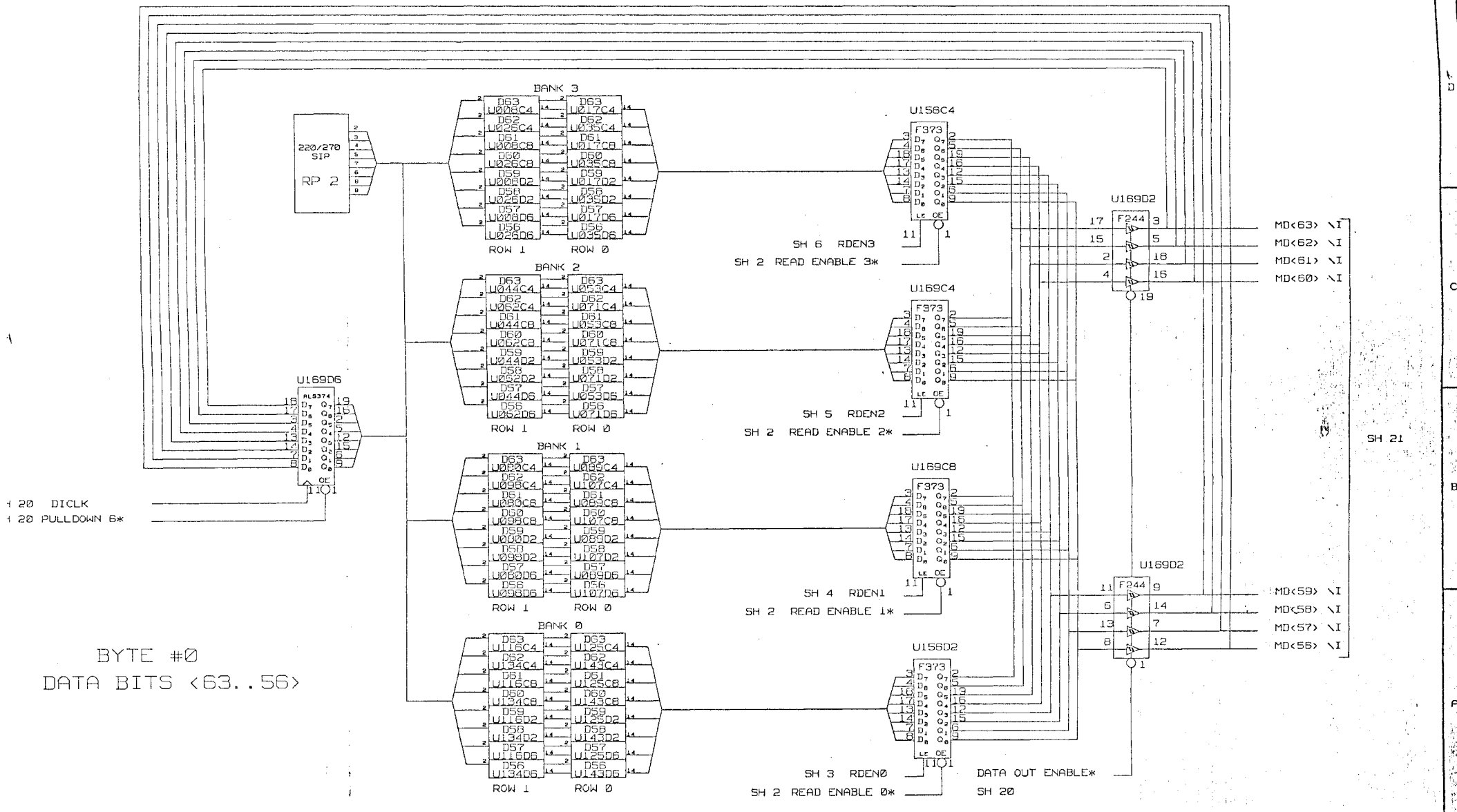
20 D1CLK  
20 PULLDOWN 5\*

BYTE #1  
DATA BITS <55..48>

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1 20 DICKL  
1 20 PULLDOWN 6\*

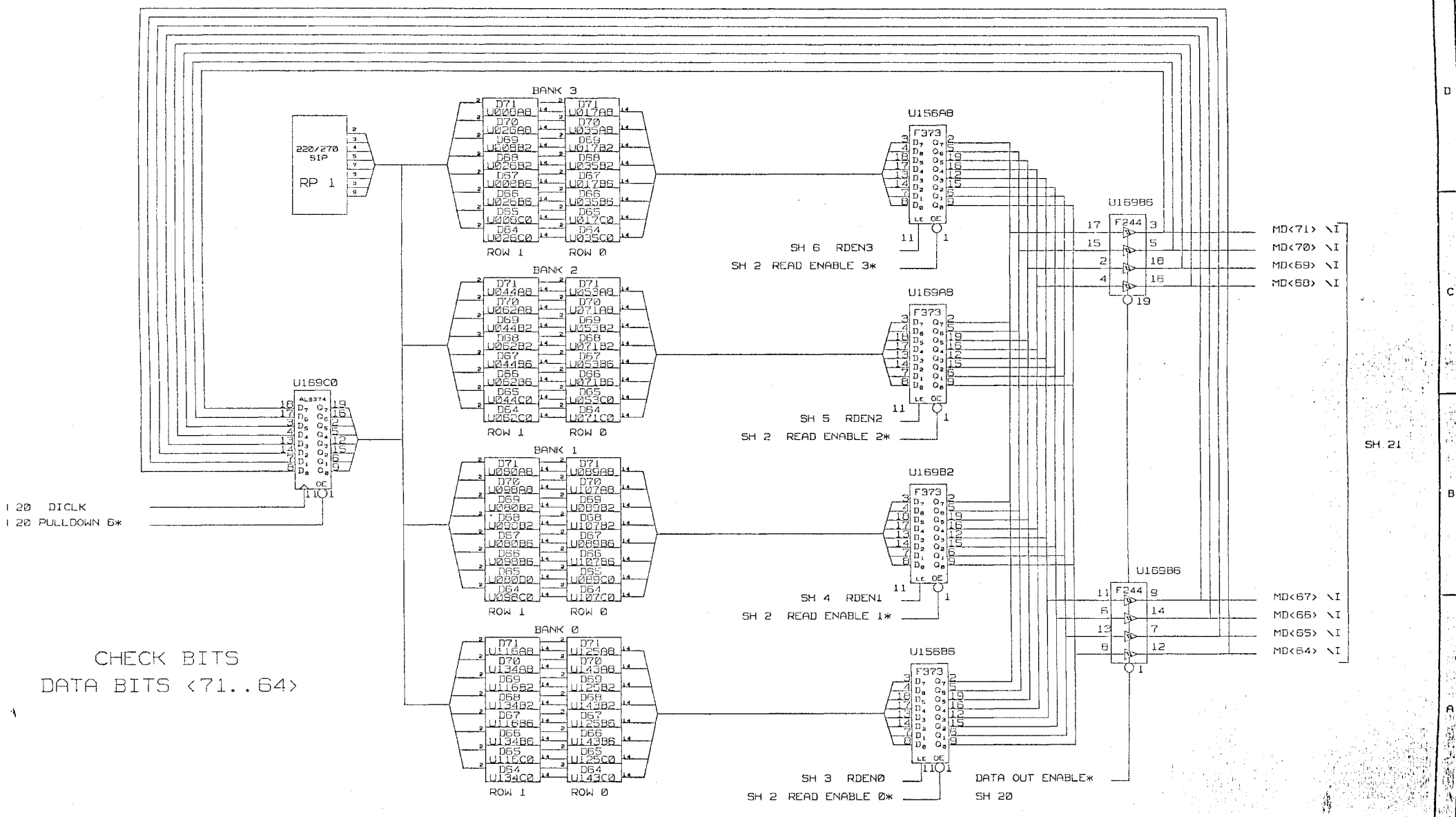
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DATA BITS <63..56>

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I 20 DICK  
I 20 PULLDOWN 6\*

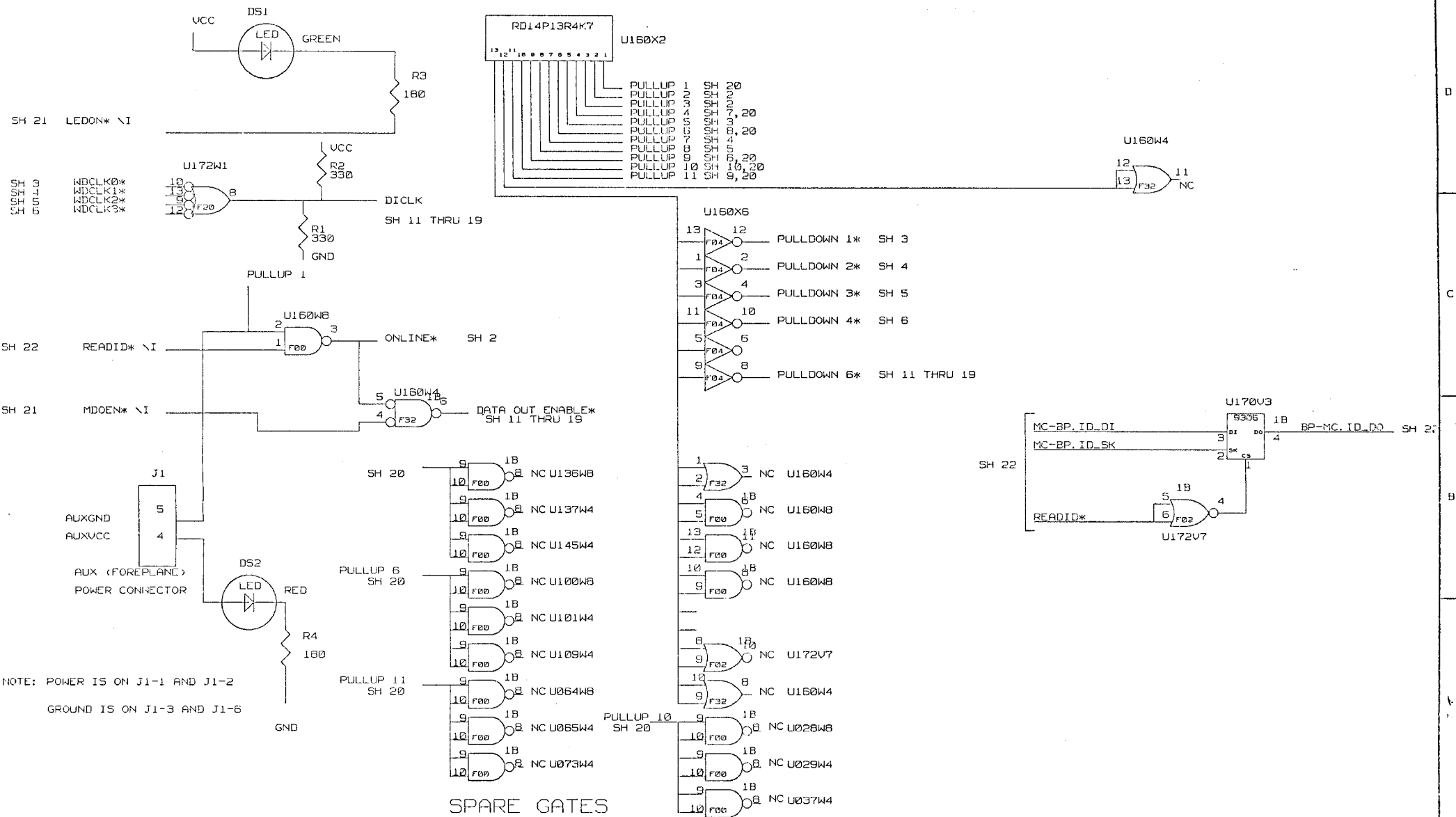
CHECK BITS  
DATA BITS <71..64>

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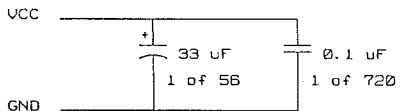
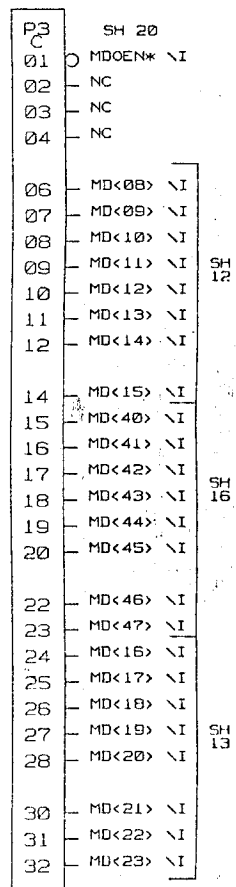
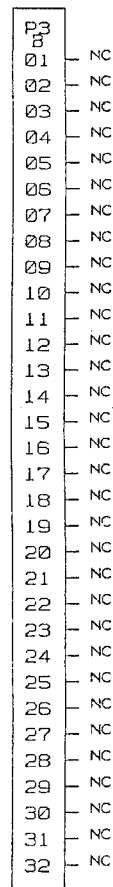
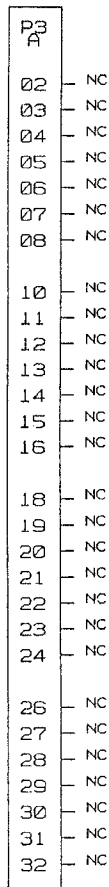
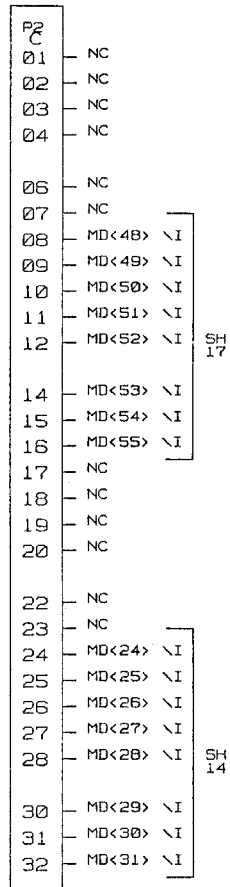
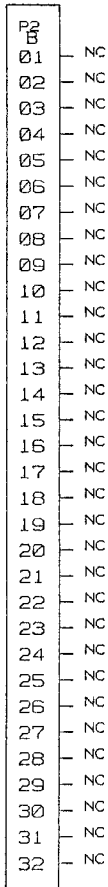
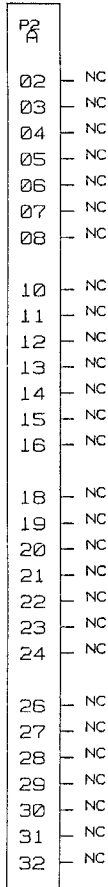
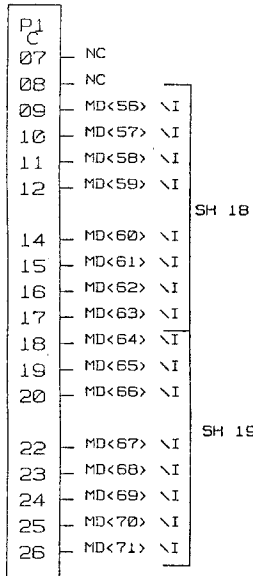
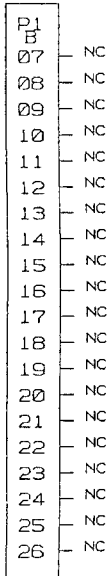
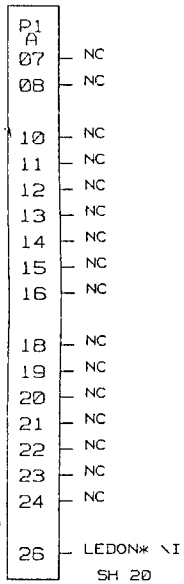


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TITLE:	MAU	REVISION:	REV 100
DRAWING:	410-000102-300	DATE:	1984.10
REVISED:	Mon Oct 29 11:11:03 1984	PAGE:	1

NOTE: Standard power and ground patterns on P1, P2, and P3 per PARSEC specification # 080-000101-000



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 REVISD: Thu Oct 11 20:08:32 1984  
 ABBR: MAU  
 ENGR: WEATHERFORD  
 PAGE: MAU, 21

P4 A
02 - NC
03 - NC
04 - NC
05 - NC
06 - NC
07 - NC
08 - NC
10 - NC
11 - NC
12 - NC
13 - NC
14 - NC
15 - NC
16 - NC
18 - NC
19 - NC
20 - NC
21 - NC
22 - NC
23 - NC
24 - NC
26 - NC
27 - NC
28 - NC
29 - NC
30 - NC
31 - NC
32 - NC

P4 B
01 - NC
02 - NC
03 - NC
04 - NC
05 - NC
06 - NC
07 - NC
08 - NC
09 - NC
10 - NC
11 - NC
12 - NC
13 - NC
14 - NC
15 - NC
16 - NC
17 - NC
18 - NC
19 - NC
20 - NC
21 - NC
22 - NC
23 - NC
24 - NC
25 - NC
26 - NC
27 - NC
28 - NC
29 - NC
30 - NC
31 - NC
32 - NC

P4 C
01 - MC-BP. ID_LSK
02 - MC-BP. ID_LDI
03 - BP-MC. ID_LDO
04 - MD<00> \I
06 - MD<01> \I
07 - MD<02> \I
08 - MD<03> \I
09 - MD<04> \I
10 - MD<05> \I
11 - MD<06> \I
12 - MD<07> \I
14 - NC
15 - NC
16 - NC
17 - NC
18 - NC
19 - NC
20 - MD<32> \I
22 - MD<33> \I
23 - MD<34> \I
24 - MD<35> \I
25 - MD<36> \I
26 - MD<37> \I
27 - MD<38> \I
28 - MD<39> \I
30 - NC
31 - NC
32 - NC

SH 20

SH 11

SH 15

P5 A
07 - MA<8> \I
08 - MA<10> \I
10 - MA<13> \I
11 - MA<15> \I
12 - MA<1> \I
13 - MA<3> \I
14 - MA<4> \I
15 - MA<6> \I
16 - MA<17> \I
18 - MRS1* \I
19 - MRFSH* \I
20 - MCI1* \I
21 - MCI3* \I
22 - MCS0 \I
23 - MCS1 \I
24 - MCS2 \I
26 - BNKEN3* \I

SH 2

SH 2

P5 B
07 - NC
08 - NC
09 - NC
10 - NC
11 - NC
12 - NC
13 - NC
14 - NC
15 - NC
16 - NC
17 - NC
18 - NC
19 - NC
20 - NC
21 - NC
22 - NC
23 - NC
24 - NC
25 - NC
26 - NC

P5 C
07 - MA<9> \I
08 - MA<11> \I
09 - MA<12> \I
10 - MA<14> \I
11 - MA<0> \I
12 - MA<2> \I
14 - MA<5> \I
15 - MA<7> \I
16 - MA<16> \I
17 - MRS0* \I
18 - MW* \I
19 - MCI0* \I
20 - MCI2* \I
22 - NC
23 - READID* \I
24 - BNKEN0* \I
25 - BNKEN1* \I
26 - BNKEN2* \I

SH 2

SH 20

SH 2

SH 2

SH 2

NOTE: Standard power and ground patterns on P4 and P5 per PARSEC specification # 080-000101-000

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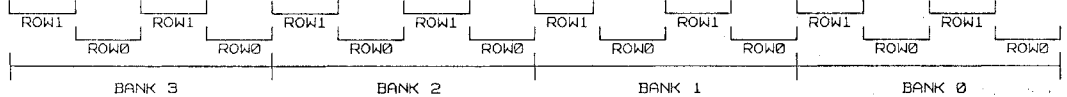
TITLE: MAU	ABBR: MAU
DRAWING: 410-000102-300 REV C00	ENGR: WEATHERFORD
REVISED: Thu Oct 11 20:10:26 1984	PAGE: MAU.22

- NOTES:
- CARD SELECTS MCS2, MCS1, AND MCS0 RESULT FROM SYSTEM ADDRESSES A26, A25, AND A24 RESPECTIVELY.
  - ROW SELECTS MRS0\* AND MRS1\* ARE A DECODE OF SYSTEM ADDRESS A23.
  - DEVICE ADDRESSES A17 THRU A0 ARE SYSTEM ADDRESSES A22 THRU A5 RESPECTIVELY.
  - BANK ADDRESSES 3, 2, 1, AND 0 ARE A DECODE OF SYSTEM ADDRESSES A4 AND A3.
  - BYTE ADDRESSES 7 THRU 0 ARE DECODES OF SYSTEM ADDRESSES A2, A1, AND A0.

	BANK 3 ADDRESS AND CONTROL LOGIC				BANK 2 ADDRESS AND CONTROL LOGIC				BANK 1 ADDRESS AND CONTROL LOGIC				BANK 0 ADDRESS AND CONTROL LOGIC				CONTROL AND ADDRESS BUFFERS
	008	017	026	035	044	053	062	071	080	088	098	107	116	125	134	143	
BYTE 7	D01	D01	D02	D02	D03	D03	D04	D04	D05	D05	D06	D06	D07	D07	D08	D08	T1
	D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	S7
	D05	D05	D04	D04	D05	D05	D04	D04	D05	D05	D04	D04	D05	D05	D04	D04	S3
BYTE 3	D07	D07	D06	D06	D07	D07	D06	D06	D07	D07	D06	D06	D07	D07	D06	D06	R9
	D33	D33	D32	D32	D33	D33	D32	D32	D33	D33	D32	D32	D33	D33	D32	D32	R5
	D35	D35	D34	D34	D35	D35	D34	D34	D35	D35	D34	D34	D35	D35	D34	D34	R1
BYTE 6	D37	D37	D36	D36	D37	D37	D36	D36	D37	D37	D36	D36	D37	D37	D36	D36	P7
	D39	D39	D38	D38	D39	D39	D38	D38	D39	D39	D38	D38	D39	D39	D38	D38	P3
	D09	D09	D08	D08	D09	D09	D08	D08	D09	D09	D08	D08	D09	D09	D08	D08	N9
BYTE 2	D11	D11	D10	D10	D11	D11	D10	D10	D11	D11	D10	D10	D11	D11	D10	D10	N5
	D13	D13	D12	D12	D13	D13	D12	D12	D13	D13	D12	D12	D13	D13	D12	D12	N1
	D15	D15	D14	D14	D15	D15	D14	D14	D15	D15	D14	D14	D15	D15	D14	D14	M7
BYTE 5	D41	D41	D40	D40	D41	D41	D40	D40	D41	D41	D40	D40	D41	D41	D40	D40	M3
	D43	D43	D42	D42	D43	D43	D42	D42	D43	D43	D42	D42	D43	D43	D42	D42	L9
	D45	D45	D44	D44	D45	D45	D44	D44	D45	D45	D44	D44	D45	D45	D44	D44	L5
BYTE 1	D47	D47	D46	D46	D47	D47	D46	D46	D47	D47	D46	D46	D47	D47	D46	D46	L1
	D17	D17	D16	D16	D17	D17	D16	D16	D17	D17	D16	D16	D17	D17	D16	D16	K7
	D19	D19	D18	D18	D19	D19	D18	D18	D19	D19	D18	D18	D19	D19	D18	D18	K3
BYTE 4	D21	D21	D20	D20	D21	D21	D20	D20	D21	D21	D20	D20	D21	D21	D20	D20	J9
	D23	D23	D22	D22	D23	D23	D22	D22	D23	D23	D22	D22	D23	D23	D22	D22	J5
	D49	D49	D48	D48	D49	D49	D48	D48	D49	D49	D48	D48	D49	D49	D48	D48	J1
BYTE 0	D51	D51	D50	D50	D51	D51	D50	D50	D51	D51	D50	D50	D51	D51	D50	D50	H7
	D53	D53	D52	D52	D53	D53	D52	D52	D53	D53	D52	D52	D53	D53	D52	D52	H3
	D55	D55	D54	D54	D55	D55	D54	D54	D55	D55	D54	D54	D55	D55	D54	D54	F9
BYTE 7	D25	D25	D24	D24	D25	D25	D24	D24	D25	D25	D24	D24	D25	D25	D24	D24	F2
	D27	D27	D26	D26	D27	D27	D26	D26	D27	D27	D26	D26	D27	D27	D26	D26	E8
	D29	D29	D28	D28	D29	D29	D28	D28	D29	D29	D28	D28	D29	D29	D28	D28	E4
BYTE 6	D31	D31	D30	D30	D31	D31	D30	D30	D31	D31	D30	D30	D31	D31	D30	D30	E0
	D57	D57	D56	D56	D57	D57	D56	D56	D57	D57	D56	D56	D57	D57	D56	D56	D6
	D59	D59	D58	D58	D59	D59	D58	D58	D59	D59	D58	D58	D59	D59	D58	D58	D2
BYTE 5	D61	D61	D60	D60	D61	D61	D60	D60	D61	D61	D60	D60	D61	D61	D60	D60	C8
	D63	D63	D62	D62	D63	D63	D62	D62	D63	D63	D62	D62	D63	D63	D62	D62	C4
	D65	D65	D64	D64	D65	D65	D64	D64	D65	D65	D64	D64	D65	D65	D64	D64	C0
BYTE 4	D67	D67	D66	D66	D67	D67	D66	D66	D67	D67	D66	D66	D67	D67	D66	D66	B8
	D69	D69	D68	D68	D69	D69	D68	D68	D69	D69	D68	D68	D69	D69	D68	D68	B2
	D71	D71	D70	D70	D71	D71	D70	D70	D71	D71	D70	D70	D71	D71	D70	D70	A8

DATA LATCHES AND BUFFERS

CONN P5  
CONN P4  
CONN P3  
CONN P2  
CONN P1



ARRAY CARD LAYOUT

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